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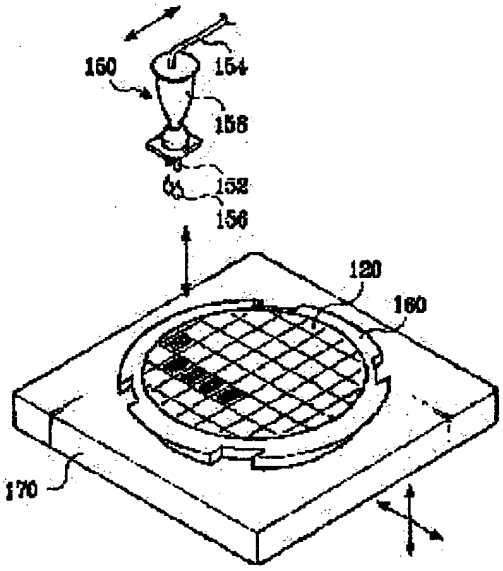
(54) LOC-TYPE SEMICONDUCTOR CHIP PACKAGE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the manufacturing cost by spreading in a wafer state a bonding agent, for bonding lead frame leads and semiconductor chips, over a lead bonding region on the semiconductor chip active surface without using a polyimide adhesive tape.
SOLUTION: In a bonding agent-applying process according to a dispensing method, firstly a wafer 120 is mounted on a x-y table 170 movable in the x and y axial directions. The x-y table 170 is moved to align a dispensing head 150 with the upper side of the wafer. When accurate alignment has been achieved, the dispensing head 150 is moved down to apply the bonding agent on a lead bonding region on the active chip surface with a needle 152. On the other hand, if the bonding agent is applied after a groove-shaped lead-bonding region is formed in the active chip surface onto which the bonding agent is to be dispensed, the overflow of the bonding agent can be prevented.



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CLAIMS

[Claim(s)]

[Claim 1] The phase of preparing the wafer which has the top in which two or more semiconductor chips which have the activity side where two or more electrode pads were arranged in the center are prepared, The phase which applies a protection layer to the top of the aforementioned wafer, and the phase which applies non-conducting adhesives to the lead adhesion field located in the both sides of the electrode pad arranged in the center of the above, The phase of dividing the aforementioned wafer into an individual semiconductor chip, and the semiconductor chip by which the separation was carried out [aforementioned] are supported. And the internal lead fraction in the leadframe which has two or more leads for connecting electrically the chip by which the separation was carried out [aforementioned] to an external circuit The die bonding phase attached in the lead adhesion field of the activity side of a semiconductor chip using the aforementioned non-conducting adhesives, The manufacture technique of LOC type semiconductor chip package equipped with the phase which connects electrically an internal lead of the aforementioned leadframe, and the electrode pad of a semiconductor chip, and the phase which forms the package fuselage which protects the aforementioned semiconductor chip.

[Claim 2] The manufacture technique of LOC type semiconductor chip package according to claim 1 possessing the phase where the phase which applies the aforementioned protection layer removes the protection layer of a predetermined position, and makes the aforementioned electrode pad and the aforementioned lead adhesion field expose and open wide.

[Claim 3] The phase where the phase which applies the aforementioned protection layer carries out spin coating of the liquefied polyimide on the top of a wafer, The phase which prepares the photo mask which has the pattern of the aforementioned electrode pad, and the pattern of the aforementioned lead adhesion field, The manufacture technique of LOC type semiconductor chip package according to claim 1 possessing the phase which applies a film on the aforementioned polyimide coating layer, the phase of using the aforementioned photo mask, and exposing and developing a film, and the phase of etching and making an electrode pad and a lead adhesion field opening wide.

[Claim 4] The manufacture technique of LOC type semiconductor chip package according to claim 1 that the phase which connects electrically an internal lead of the aforementioned leadframe and the electrode pad of a semiconductor chip is performed by wirebonding.

[Claim 5] The manufacture technique of LOC type semiconductor chip package according to claim 1 which is the adhesives with which the aforementioned non-conducting adhesives were chosen out of the group which consists of a polyimide, epoxy, a polyimide siloxane, and a polyeth r amide.

[Claim 6] The phase where the phase which applies the aforementioned non-conducting adhesives prepares for the position corresponding to the aforementioned lead adhesion field the metal screen which has an open section pattern, The phase of carrying out alignment of the aforementioned screen to the aforementioned wafer, and sticking the screen on the top of a wafer, The phase which is made to pass liquefied adhesives through the open section pattern of the aforementioned metal screen, and applies liquefied adhesives to a lead

adhesion field, The manufacture technique of LOC type semiconductor chip package according to claim 1 or 2 possessing the phase of separating the aforementioned screen from a wafer, and the phase of stiffening the liquefied adhesives applied to the aforementioned lead adhesion field.

[Claim 7] The phase where the phase which applies the aforementioned non-conducting adhesives equips with the aforementioned wafer xy table which can move to x and y shaft orientations, The phase which carries out alignment of the dace ********** head equipped with the needle which carries out dace ********** of the liquefied non-conducting adhesives of a constant rate to the wafer bottom, The manufacture technique of LOC type semiconductor chip package according to claim 1 which possesses the phase which carries out dace ********** of the aforementioned non-conducting adhesives, and the phase of stiffening the adhesives by which dace ********** was carried out [aforementioned], to the lead adhesion field of the activity side of a semiconductor chip.

[Claim 8] The manufacture technique of LOC type semiconductor chip package according to claim 7 that the aforementioned protection layer is removed alternatively and the aforementioned lead adhesion field was made to have the shape of a quirk according to a photo etching process.

[Claim 9] The manufacture technique of LOC type semiconductor chip package according to claim 7 that dace ********** of the aforementioned liquefied non-conducting adhesives is performed one by one to two or more aforementioned semiconductor chips.

[Claim 10] The manufacture technique of LOC type semiconductor chip package according to claim 7 that dace ********** of the aforementioned liquefied non-conducting adhesives is performed at a stretch to the semiconductor chip in the same line (the same train or the same line) in the aforementioned wafer.

[Claim 11] The manufacture technique of LOC type semiconductor chip package according to claim 7 that the aforementioned dace ********** head has two or more needles, and dace ********** is performed at a stretch to two or more semiconductor chips.

[Claim 12] The manufacture technique of LOC type semiconductor chip package according to claim 7 which is the adhesives with which the aforementioned non-conducting adhesives were chosen out of the group which consists of a polyimide, epoxy, a polyimide siloxane, and a polyether amide.

[Claim 13] The phase of equipping with masking tape at the rear face of the aforementioned wafer before the phase which applies the aforementioned non-conducting adhesives, It has the phase which carries out scribing of the tape insertion wafer along with the scribe line defined between the semiconductor chips which adjoin on a wafer. The phase where the phase which applies the aforementioned non-conducting adhesives equips with the aforementioned wafer xy table which can move to x and y shaft orientations, The phase which carries out alignment of the dace ********** head equipped with the needle which carries out dace ********** of the liquefied non-conducting adhesives of a constant rate to the wafer bottom, The manufacture technique of LOC type semiconductor chip package according to claim 1 which equips the lead adhesion field of the activity side of a semiconductor chip with the phase which carries out dace ********** of the aforementioned non-conducting adhesives, and the phase of stiffening the adhesives by which dace ********** was carried out [aforementioned].

[Claim 14] The manufacture technique of LOC type semiconductor chip package according to claim 13 which is the phase of removing the specific semiconductor chip chosen from the masking tape attached in the rear face of the aforementioned wafer by pushing up the specific selected semiconductor chip from the wafer with which dace ********** of the aforementioned non-conducting adhesives is carried out, and the aforementioned xy table is equipped with the phase of dividing the aforementioned wafer into an individual semiconductor chip.

[Claim 15] The manufacture technique of LOC type semiconductor chip package according to claim 13 which recognizes the poor chip identification display as which the phase which carries out dace ********** of the non-conducting adhesives is displayed on the lead

adhesion field of the a ity side of the aforementioned semic ductor chip by the semiconductor chip on a wafer, and possesses the phase of performing dace ********** alternatively only to the semiconductor chip which does not have this display.
[Claim 16] The semiconductor chip which has the activity side where two or more electrode pads are arranged in the center, The leadframe which has the lead attached in the activity side of the aforementioned semiconductor chip, The electric link means for connecting electrically a lead of the aforementioned leadframe, and the electrode pad of the aforementioned semiconductor chip, It has a package fuselage for protecting the aforementioned semiconductor chip, a lead, and an electric link means. The activity side of the aforementioned semiconductor chip has a lead adhesion field in the position in which the aforementioned lead should be attached. in the aforementioned lead adhesion field LOC type semiconductor chip package to which the adhesives which are made to apply and harden liquefied non-conducting adhesives in the wafer status before separating an individual semiconductor chip from a wafer, and were formed are applied.
[Claim 17] the field for making the field for the protection layer equipped with an inactive layer and a polyimide coating layer being applied to the aforementioned activity side, and the aforementioned protection layer making the aforementioned electrode pad open wide, and the aforementioned lead adhesion field open wide -- having -- in addition -- and LOC type semiconductor chip package according to claim 16 whose aforementioned lead adhesion field has the shape of a quirk
[Claim 18] The aforementioned non-conducting adhesives are LOC type semiconductor chip packages according to claim 16 which are the adhesives chosen out of the group which consists of a polyimide, epoxy, a polyimide siloxane, and a polyether amide.
[Claim 19] The phase of preparing the metal screen to which the aforementioned non-conducting adhesives have an open section pattern in the position corresponding to the aforementioned lead adhesion field, The phase of carrying out alignment of the aforementioned screen to the aforementioned wafer, and sticking the screen on the top of a wafer, The phase which is made to pass liquefied adhesives through the open section pattern of the aforementioned metal screen, and applies liquefied adhesives to a lead adhesion field, LOC type semiconductor chip package according to claim 16 formed of the process equipped with the phase of separating the aforementioned screen from a wafer, and the phase of stiffening the liquefied adhesives applied to the aforementioned lead adhesion field.
[Claim 20] The phase where the aforementioned non-conducting adhesives equip with the aforementioned wafer xy table which can move to x and y shaft orientations, The phase which carries out alignment of the dace ********** head equipped with the needle which carries out dace ********** of the liquefied non-conducting adhesives of a constant rate to the wafer bottom, LOC type semiconductor chip package according to claim 16 formed in the lead adhesion field of the activity side of a semiconductor chip of the process equipped with the phase which carries out dace ********** of the aforementioned non-conducting adhesives, and the phase of stiffening the adhesives by which dace ********** was carried out [aforementioned].
[Claim 21] It is LOC type semiconductor chip package according to claim 20 scribing of the wafer is carried out [package] to an individual semiconductor chip along with the scribe line defined between adjoining semiconductor chips by the tape for protection having pasted the rear face of the wafer with which the aforementioned xy table is equipped.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] More specifically, this invention relates to LOC type semiconductor chip package in which the adhesives for pasting up a semiconductor chip and a lead of a leadframe are applied and formed in the lead adhesion field of the activity side of a semiconductor chip in the state of a wafer, and its manufacture technique about LOC (Lead-On-chip) type semiconductor chip package.
[0002]
[Description of the Prior Art] A package has the structure attached in the lead fraction of a leadframe instead of LOC type semiconductor chip attaching a semiconductor chip in a leadframe pad (die pad). Since a leadframe lead must be electrically connected to a semiconductor chip, an internal lead fraction is attached in the activity side of a chip in which the electrode pad is prepared. Then, a lead is arranged at the semiconductor chip bottom, as shown in drawing 12 . That is, if drawing 12 is referred to, the leadframe 10 containing the internal lead 12, the external lead 14, and the bus bar 16 will be pasted up on the top of a semiconductor chip with adhesives 30. A leadframe 10 consists of a copper alloy or an iron alloy. Adhesives 30 paste up the internal lead 12 and the bus bar 16 on the activity side 24 of a semiconductor chip established in the electrode pad 22, and the between semiconductor chip like an erector carries out the role supported by the leadframe.
[0003] The internal lead 12 and the electrode pad 22 are electrically connected by the bonding wire 40 of gold or aluminum, as shown in drawing 13 . A bus bar 16 is the lead for supplying power to a semiconductor chip 20 stably. If the external lead 14 projected from the fuselage is bent in the suitable gestalt, for example, a J character configuration, after forming the package fuselage for protection 50, LOC type package will be obtained.
[0004] With such LOC type package technique, since the ratio of the size of a semiconductor chip and a package size can be raised, a manufacture of a compact-package element is attained. For example, with the package element which has general structure, although the ratio of a package size and a chip size is a maximum of 70% with COL (Chip-On-Lead) type package a maximum of 60%, in the case of LOC type package, a size ratio can be raised a maximum of 90%. Moreover, with LOC type package, since it has the advantage that the reliability fall resulting from the differentiation in the physical property between different-species matter, for example, the differentiation in the coefficient of thermal expansion between a package fuselage and a leadframe etc., can be prevented in order not to use a leadframe pad, the semiconductor manufacturer of present [many] uses.
[0005] Although the polyimide system double faced adhesive tape by which polyimide film both sides were usually coated with adhesives, for example, thermosetting epoxy adhesives, is used as adhesives 30 used for LOC type package, the manufacture process is as follows. First, the adhesives of the melting status are uniformly applied to the whole surface of a polyimide film by fixed thickness. And it is made to harden so that adhesives may be in the semisolid status. subsequently, on the other hand, a polyimide film is alike similarly, and the adhesives of the melting status are applied and stiffened After cutting the polyimide tape on which adhesives were applied so that it may have fixed width of face, it is transported to the die bonding process which attaches a semiconductor chip and a leadframe.

[0006] Drawing 14 A c[redacted]rawing 14 C is a fragmentary sectio[redacted]iew for explaining the process in which a semiconductor chip is pasted up on a leadframe using the aforementioned polyimide tape. Adhesives 30 are attached in a leadframe 10 by sticking a leadframe 10 and the adhesives 30 equipped with the internal lead 12 and the bus bar 16 by pressure, applying about 200 or 400-degree C heat by the heater 60 and the punching machine 70. In this case, the punching of the unnecessary fraction of adhesives is carried out, and a punching machine 70 removes it so that the gestalt of a leadframe may be suited. A semiconductor chip 20 is laid on the heater block 80, and a tape is pasted up on the activity side of a semiconductor chip.
[0007] However, LOC type semiconductor chip package element by such conventional technique has the following troubles.
[0008] Since the manufacturing process is complicated, the polyimide tape of a three-tiered structure on which adhesives are applied in the first place at both sides has a limitation in causing the elevation for manufacturing costs and minimizing the thickness of a tape.
[0009] The process which attaches a polyimide tape in the second at a lead of a leadframe becomes the factor as which the working limit of a punching machine determines the minimum size of adhesives in order to use the mechanical manipulation technique by the punching method, and the burr (burr) of the tape mostly generated in a punching process has a possibility of causing a failure as a future erector.
[0010] Since the polyimide tape touches the leadframe which is the different-species matter, the semiconductor chip, and the plastic-package fuselage, it may cause the failure of a package in the third by the thermal stress resulting from the differentiation in the coefficient of thermal expansion between the reliability checks conducted under an elevated temperature and the humid ambient atmosphere, and between different-species matter. Moreover, since a polyimide film and adhesives have high hygroscopicity, when a package is mounted in an external circuit substrate by soldering, they can cause a package crack.
[0011] Therefore, the policy which suppresses the elevation for manufacturing costs in order to apply LOC package technique, and the policy which decreases the size and thickness of a tape in order to conquer the reliability fall by the contact between different-species matter are needed.
[0012]
[Problem(s) to be Solved by the Invention] Therefore, the purpose of this invention is to offer LOC type semiconductor chip package element which can reduce the object for manufacturing costs, and its manufacture technique.
[0013] It is in other purposes of this invention raising the reliability of LOC type semiconductor chip package.
[0014]
[Means for Solving the Problem] The manufacture technique of LOC type semiconductor chip package by this invention applies liquefied non-conducting adhesives to the lead adhesion field of the activity side of a semiconductor chip in the state of a wafer, before not using the adhesives of the tape gestalt and separating a semiconductor chip from a wafer individually, in order to attach a lead and semiconductor chip of a leadframe. When applying liquefied adhesives in the state of a wafer, in order to prevent that adhesives overflow to the activity side of semiconductor chips other than a lead adhesion field, a lead adhesion field is formed so that it may have the shape of a quirk. The mask used in order to make an electrode pad open wide from protection layers, such as an inactive layer applied on an activity side and a polyimide coating layer, after completing a manufacture of a semiconductor chip by wafer manipulation can be used for the lead adhesion field of the shape of this quirk as it is, and it can attain it by including the pattern for a lead adhesion field in this mask.
[0015] The technique of applying adhesives in the state of a wafer arranges and carries out alignment of the screen which has a desired pattern corresponding to a lead adhesion field to the wafer bottom. or [using the screen printing with which liquefied adhesives are applied to the lead adhesion field of the activity side of the semiconductor chip of the wafer status by the squeegee (squeegee) through a lead adhesion field pattern, after sticking a wafer and the

screen] -- or The lead adhesion field of the activity side of a semiconductor chip is recognized in the state of a wafer, and it is a wire dispenser (dispenser). The dace ********** (dispensing) method which uses and applies liquefied adhesives to this field can be used.

[0016] When using the dace ********** method, adhesives may be applied to a target one by one to the semiconductor chip on a wafer, and dace ********** may be applied at a stretch to many semiconductor chips. Moreover, if a dace ********** head is included in die bonding equipment equipped with the system which recognizes the position of the semiconductor chip on a wafer, and xy table which can move a wafer to xy shaft orientations, a dace ********** process can be advanced more efficiently.

[0017]

[Embodiments of the Invention] Hereafter, this invention is more explained to a detail, referring to a drawing.

[0018] The manufacture technique of LOC type semiconductor chip package by this invention is advanced according to the flow chart showing in drawing 1 fundamentally. Two or more semiconductor chips which have a desired capacity and a desired function in a wafer manufacture phase (100) are batch processes (batch process). It is manufactured simultaneously. In the semiconductor chip used for LOC type package, the electrode pad is arranged at a part for the center section of the activity side in which the circuit element is prepared, and a lead of a leadframe is attached in the activity side of this chip.

[0019] Although a protection layer is covered on a wafer after a manufacture of a circuit element finishes (phase 102), a protection layer may be an inactive layer generally used by the semiconductor manufacturing process, and may be a polyimide layer coated on this inactive layer. A polyimide coating layer carries out the role from which the activity side of a semiconductor chip is protected at the time of the rear-face polishing process which grinds the rear face of a wafer in order to make thickness of a wafer thin, and an inactive layer is protected at the time of the forming cycle which forms a package fuselage. Moreover, since a polyimide coating layer has the function to reduce SER (soft error ratio) by the alpha particle emitted from the activity matter contained in the package fuselage, it is broadly used by the present semiconductor manufacturing process. A polyimide layer is mainly coated by the spin coating method.

[0020] although applied to the whole activity side of a wafer, in this case, the electrode pad of a semiconductor chip is opened wide, and if there is no protection layer, it will not become This electrode pad is because it acts as a path which makes a semiconductor chip connect outside electrically and a wire must connect with a leadframe between wirebonding processes. The open phase (103) of an electrode pad is performed using a general etching process. On the other hand, although it mentions later for details when opening an electrode pad, it is desirable that the field where adhesives are applied to the activity side of a semiconductor chip, i.e., a lead adhesion field, is opened wide together, and a lead adhesion field is made to have the shape of a quirk.

[0021] Adhesives are applied to the lead adhesion field on the front face of a wafer where the protection layer was applied (phase 104), and a semiconductor chip is individually separated from a wafer (105). The semiconductor chip separated with the individual element is attached in a leadframe lead (106). The semiconductor chip separated from the wafer is called 'die', and it is called die bonding to attach this die in a leadframe. In the die bonding phase 106, the adhesives applied to the front face of a semiconductor chip are used between phases 104, without using special adhesive tape.

[0022] A future process cuts the wirebonding process (107) which connects electrically a leadframe lead and the electrode pad of a semiconductor chip, the closure phase (108) which forms a protection package fuselage, a protection package fuselage, and a lead from a leadframe strip as similarly as a common package erector, and advances in the order of disconnection/bending phase (109) which bends the lead fraction projected from the package fuselage with the suitable gestalt.

[0023] The drawing 2 or the drawing 4 is the perspective diagram and partial enlarged view for

explaining the process which forms the lead adhesion field of shape of a quirk by this invention.
[0024] A lead adhesion field is formed in the electrode pad opening phase (103) of drawing 1 . The electrode pad opening field 124 and the lead adhesion field 122 can be formed using the photo mask 110 generally used on the conventional general photolithography (photolithography) technique. Chromium 116 is formed in the glass plate by the fixed pattern at the photo mask. The lead adhesion field pattern 112 and the electrode pad opening pattern 114 are contained in this mask pattern.
[0025] A film is covered on the whole front face of the wafer 120 with which the protection layer 128 is applied, and the mask 110 with which patterns 112 and 114 are formed in the bottom is aligned. If light, such as a ultraviolet radiation, is irradiated on the surface of a wafer through a mask 110, as for the film applied to the wafer front face, in response to light, the chemical property will change with mask patterns partially. If it is exposed and a part for a protection layer is etched after removing the fraction which developed the wafer and received the light in a film, the lead adhesion field 122 and the electrode pad opening field 124 which were shown in drawing 4 will be formed. Since the lead adhesion field 122 has the shape of a quirk, when applying adhesives to this field 122 by this invention, the application of adhesives is easy for it and it can prevent overflow of adhesives. However, it is possible to apply direct adhesives not on the thing which must form the lead adhesion field 122 in the protection layer 128 but on the protection layer 128, and to also make it paste up with a leadframe lead.
[0026] There is various technique as the technique of applying adhesives to the specific field, i.e., the lead adhesion field, of an activity side of a semiconductor chip in the state of a wafer. Among those, it is the technique in which the spin coating method rotates liquefied adhesives after optimum-dose ********, and rotates a wafer on the surface of a wafer at high speed, and liquefied adhesives are made to spread all over a wafer with a centrifugal force. although it has the advantage in which time to apply adhesives to a wafer front face is short, since adhesives are not applied only to a lead adhesion field and applied to the whole wafer front face, after stiffening the applied adhesives, this opens an electrode pad wide, and if there is nothing, it will not become However, in order to secure the stable adhesion between a semiconductor chip and a lead between die bonding processes and to protect the activity side of a chip, you have to apply the adhesives layer which has the thickness of about 30 micrometers or more. Therefore, much time becomes such a thing at the etching process for electrode pad opening. Moreover, in order that a thick adhesives layer may cover the whole electrode pad, it also becomes causing waste of money of adhesives and causing the reliability fall resulting from the differentiation in the coefficient of thermal expansion with other matter, for example, a silicon chip, or a package fuselage.
[0027] Drawing 5 is a perspective diagram for explaining the process which applies adhesives to the lead adhesion field of the semiconductor chip of the wafer status using the screen printing by this invention.
[0028] The open section pattern 132 for the screen 130 which consists of a metallic foil applying adhesives 140 to the lead adhesion field 122 established in the chip activity side of a wafer 120 is formed. The alignment key (not shown) for the exact alignment with a wafer 120 is prepared in the screen 130. After alignment finishes, the screen 130 and the wafer 120 are stuck. Therefore, only the lead adhesion field 122 on a wafer is exposed outside with the pattern 132. Adhesives 140 will be applied to the lead adhesion field 122 if a squeegee 134 is moved in the orientation of the arrow head, supplying the liquefied adhesives 140 on the screen. The screen 130 is removed after an adhesives application and adhesives are stiffened. The last structure is as being shown in drawing 6 A and drawing 6 B. Drawing 6 A is the partial enlarged view showing the structure where adhesives 142 are applied to the semiconductor chip 126 by the screen printing, and drawing 6 B is the cross section cut along with the line 6-6 of drawing 6 A.
[0029] Adhesives should consist of the non-conducting matter and any one, a polyimide, epoxy, a polyimide siloxane, and the polyether amide, can be used for them. As for adhesives, what is excellent in viscosity or a thixotropy is desirable. In the case of epoxy adhesives, a

curing temperature is somewhat higher than other adhesives.
[0030] Although the advantage in which adhesives can be once applied to two or more lead adhesion fields by work is in a screen printing, the adhesives used for this process must bear so long working hours. Adhesives are strike wringings (stringing) in carrying out the trap of the air too much ****. It must cause, or it bends and must be designed like and pertinently. If adhesives are applied with a screen printing, since the pattern and thickness of adhesives which are formed are easily controllable by the design change of the screen, the failure of LOC type package by use of the conventional adhesives can be abolished. When advancing work continuously to two or more wafers with the one screen, you have to remove the adhesives attached to the screen rear face in contact with a wafer. Moreover, since the applied adhesives layer may form a non-flat-surface-like wafer side inevitably and this may cause trauma to a wafer in the tape package phase over a wafer side, in a future assembly phase, a wafer must be dealt with carefully.
[0031] Drawing 7 is an outline perspective diagram for explaining the process which applies adhesives to the lead adhesion field of the semiconductor chip of the wafer status by the dace ********** method.
[0032] It equips with the wafer 120 currently fixed with the wafer ring 160 on the xy table 170 which can move to x and y shaft orientations. The dace ********** head 150 is equipped with the tube 154 which supplies the liquefied adhesives 156, the syringe 158 containing the adhesives of a constant rate, and two or more needles 152 which carry out dace ********** of the adhesives.
[0033] As mentioned above, any one, the polyimide which is the non-conducting matter, epoxy, a polyimide siloxane, and the polyether amide, is used for adhesives. The position of the lead adhesion field of a chip activity side is recognized using an optical system (not shown), by controlling drive meanses, such as a stepping motor or a servo motor, based on this recognition information, moves the xy table 170 and carries out alignment of the dace ********** ********** head to the wafer bottom. If exact alignment is made, a dace ********** head will down and adhesives will be applied to the lead adhesion field of a chip activity side through a needle. After the adhesives application to one semiconductor chip finishes, a dace ********** head goes up, the xy table 170 is moved, and alignment of the following semiconductor chip is carried out. When carrying out dace ********** of the adhesives through a needle, the amount of adhesives can be controlled by the pneumatic pressure.
[0034] Overflow of adhesives can be prevented if adhesives are applied on the other hand after forming the lead adhesion field 124 of the shape of a quirk explained while referring to drawing 4 in the chip activity side where dace ********** of the adhesives is carried out.
[0035] Since the application of adhesives is possible for such a dace ********** method, without a dace ********** head touching a wafer front face directly, compared with the screen printing, the handling with a wafer stable regardless of thickness, a size, etc. of a wafer is possible for it. And since the width of face of the adhesives with which adhesives are applied [with which are applied and it is application-located] by changing the diameter of a needle and the motion speed of a head and controlling a pneumatic pressure, a length, and thickness are easily controllable, in the structure of LOC type package, or the field of a reliability, selection of optimal structure is possible.
[0036] the application of the adhesives by dace ********** was mentioned above -- as -- one semiconductor chip of the wafer status -- receiving -- every [once] -- adhesives, although dace ********** can also be advanced It is a long line (long line) to two or more semiconductor chips which are in the same line as shown in drawing 8 . As it is also possible to carry out dace ********** (156a) of the adhesives in a format or it is shown in drawing 9 It is also possible to equip one dace ********** head 180 with the multi-needles 152a, 152b, 152c, and 152d, and to carry out dace ********** (156b) of the adhesives simultaneously to two or more semiconductor chips. Moreover, thickness of adhesives can be made regularity if dace ********** is simultaneously advanced to two or more semiconductor chips. Furthermore, since scribing by the diamond wheel which rotates with a high rotational speed in a wafer disconnection phase is performed even if it carries out day

pen ****** of the ad ves and it applies them in a long line mat to the chip in the same line, as for an adjoining semiconductor chip, what are separated easily satisfactory.
[0037] Until now, it explained using a special dace ********** machine for the lead . adhesion field of the semiconductor chip of the wafer status, when carrying out the De Dis ** ******* of the adhesives. This dace ********** machine must be equipped with the optical system for recognizing the position of the drive means for moving the table on which it was equipped with the wafer to xy shaft orientations, and the lead adhesion field of a semiconductor chip etc. On the other hand, the conventional die bonding equipment is equipped with xy table to which a wafer can be moved, and the optical system which recognizes the position of the specific semiconductor chip on a wafer. Therefore, if a dace ********** head is included in the conventional die bonding equipment, compaction of a cost saving or process time can be aimed at.
[0038] Drawing 10 is a schematic diagram of a die bonding equipment equipped with the dace ********** head 150.
[0039] The semiconductor wafer 120 currently fixed to the wafer ring 160 passes through a wafer side polishing phase, a masking tape package phase, and a wafer disconnection (that is, scribing) phase further through a wafer manufacture phase (100 of drawing 1), a protection stratification phase (102), and an electrode pad opening phase (103). Although the scribe of the wafer 120 is carried out to each semiconductor chip, a chip is supported with the masking tape 220 attached in the rear face. If a wafer 120 is laid in the extended table 190 and a tape 220 is pulled outside using the extended ring 192, the semiconductor chip by which scribing was carried out will place and leave distance to some extent. Since it is combined with the xy table 200, the extended table 190 is movable to x and y shaft orientations. The optical system 240 is CCD (charge coupled device). It has a camera 242 and the monitor 244. A camera 242 recognizes the position of the specific semiconductor chip on the wafer 120 with which the xy table 200 is equipped, and outputs this positional information to a monitor 244. The positional information of the optical system 240 is used for carrying out alignment of the pickup tool 230 and the dace ********** head 150 on a wafer at the same time it is used for controlling the drive motor (not shown) which makes the xy table 200 drive.
[0040] After carrying out alignment of the dace ********** head 150 on a wafer, the non-conducting liquefied adhesives which were contained in the syringe 158 through the tube 154 of a head 150 are applied to the lead adhesion field of a chip activity side from a needle 152 by the pneumatic pressure supplied from the air tube 155. In this case, dace ********** may advance a target one by one for every semiconductor chip, or may be simultaneously advanced to two or more semiconductor chips. On the other hand, it is common to give ink dotting on the front face of the poor chip between EDS (Electrical Die Sorting) checks and on a wafer 120. Therefore, if the dace ********** method which applies adhesives is used after recognizing an individual chip, since adhesives will not be applied to a poor chip unlike spin coating or a screen printing, futility ****** of adhesives can be prevented.
[0041] An individual chip is completely separable from a tape 220 120, i.e., a wafer, by the ejector 210 which has a knock out pin (not shown) moving to a position P1 after an application of adhesives, and hardening, and pushing up the selected individual chip. The separated chip is moved to die bonding equipment with the pickup tool 230.
[0042] Drawing 11 is a partial schematic diagram of the die bonding equipment for explaining the process which carries out bonding of the individual semiconductor chip 290 and the leadframe.
[0043] The leadframe 280 of a strip configuration moves in the arrow head A1 orientation along with the migration rail 270. The leadframe 280 is equipped with the internal lead 282, the external lead 284, and the bus bar 286, and bonding of an internal lead and the bus-bar fraction will be carried out to a semiconductor chip 290 by the adhesives 156 applied to the activity side of a semiconductor chip 290 by this invention.
[0044] The pickup tool 230 carries the individual semiconductor chip 290 along with an arrow head A 2-way, and lays in the die bonding position of the heater block 260. The vertical move is possible for the heater block 260 as the arrow head A4 shows. If a leadframe 280 moves

along with the arrow he[redacted]A1 and arrives at a die bonding positi[redacted], bonding of the leadframe lead will be carri d out to the activity side of a semiconductor chip by carrying out thermocompression bonding of the semiconductor chip to a lead of a leadframe with the die bonding head 250 and the heater block 260. Although adhesives are applied to a leadframe pad with the conventional general package in a position P2, as mentioned above, adhesives 156 are already applied to the lead adhesion field of a chip activity side with LOC type package by this invention.

[0045]

[Effect of the Invention] As explained above, since the adhesives for LOC type package element by this invention pasting up a leadframe lead and a semiconductor chip are applied to the lead adhesion field of a semiconductor chip activity side in the state of a wafer, the polyimide adhesive tape which consists of a three-tiered structure does not need to be used for them. Therefore, since the object for manufacturing costs can be reduced and a size, thickness, etc. of adhesives can be adjusted easily, the reliability of a package element can be raised.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the flow chart of the manufacturing process of LOC type semiconductor chip package by this invention.
[Drawing 2] It is the perspective diagram showing the photo mask used in order to form the lead adhesion field of the shape of a quirk by this invention at the same time it opens an electrode pad from a protection layer.
[Drawing 3] It is the partial enlarged view of the photo mask which has an electrode pad pattern and a lead adhesion field pattern.
[Drawing 4] It is the partial enlarged view showing the chip activity side in which the electrode pad opening field and the lead adhesion field of the shape of a quirk by this invention were formed.
[Drawing 5] It is a perspective diagram for explaining the process which applies adhesives to the lead adhesion field of the semiconductor chip of the wafer status using the screen printing by this invention.
[Drawing 6] Drawing 6 A is the partial expansion perspective diagram showing the structure of the semiconductor chip of the wafer status that adhesives were applied by the screen printing by this invention, and drawing 6 B is the fragmentary sectional view.
[Drawing 7] It is an outline perspective diagram explaining the process which applies adhesives to the lead adhesion field of the semiconductor chip of the wafer status by the dace ********** method.
[Drawing 8] It is the outline perspective diagram showing the process which carries out dace ********** of the adhesives in a long line format to the lead adhesion field of two or more semiconductor chips which are in the same line especially by the dace ********** method in the process which applies adhesives.
[Drawing 9] It is the outline perspective diagram showing the process which performs dace ********** simultaneously to two or more chips using the dace ********** head which has two or more needles especially by the dace ********** method in the process which applies adhesives.
[Drawing 10] It is the schematic diagram of die bonding equipment equipped with a dace ********** head.
[Drawing 11] It is the partial schematic diagram of the die bonding equipment explaining the process which carries out bonding of an individual semiconductor chip and an individual leadframe.
[Drawing 12] It is the perspective diagram showing the structure of the conventional LOC type semiconductor chip package.
[Drawing 13] It is the transverse-plane cross section showing the structure of the conventional LOC type semiconductor chip package.
[Drawing 14] It is the fragmentary sectional view showing the conventional process of attaching a leadframe in the activity side of a semiconductor chip using a polyimide tape.
[Description of Notations]
110 Photo Mask
112 Lead Adhesion Field Pattern
114 Electrode Pad Opening Pattern

116 Chromium
120 Wafer
122 Lead Adhesion Field
124 Electrode Pad Opening Field
126 Semiconductor Chip
128 Protection Layer
130 Screen
132 Open Section Pattern
134 Squeegee
140 Adhesives
142 Adhesives
150 Dace ********** Head
152 Needle
152a, 152b, 152c, 152d Multi-needle
154 Tube
155 Air Tube
156 Adhesives
158 Syringe
160 Wafer Ring
170 Xy Table
180 Dace ********** Head
190 Extended Table
192 Extended Ring
200 Xy Table
210 Ejector
220 Tape
230 Pickup Tool
240 Optical System
242 CCD Camera
244 Monitor
250 Die Bonding Head
260 Heater Block
270 Migration Rail
280 Leadframe
282 Internal Lead
284 External Lead
286 Bus Bar
290 Semiconductor Chip

[Translation done.]